CLAIMS

1. A nonvolatile memory device with simultaneous read/write, comprising:

a memory array, having a plurality of cells organized into memory banks; and

a plurality of first sense amplifiers;

a plurality of second sense amplifiers;

a plurality of R/W selectors associated with respective sets of said cells and connecting said cells of said respective sets of said cells alternately to said first sense amplifiers and to said second sense amplifiers.

2. The device according to claim 1, wherein each of said memory banks comprises a respective plurality of said R/W selectors.

3. The device according to claim 1, wherein said memory banks comprise respective local decoding branches, each local decoding branch being connected to a respective one of said R/W selectors.

4. The device according to claim 3, wherein each of said local decoding branches comprises at least one first local decoder and a plurality of local bitlines, connected to said first local decoder.

5. The device according to claim 4, wherein each of said local decoding branches comprises a plurality of said first local decoders and at least one second local decoder, connected to said first local decoders and to the respective said R/W selector.

6. The device according to claim 1, wherein said R/W selectors can be controlled independently of one another.

7. The device according to claim 1, wherein said R/W selectors belonging to a same of said memory banks are controlled in phase.

8. The device according to claim 1, further comprising:

first and second global bitlines connecting said R/W selectors to said first and, respectively, to said second sense amplifiers.

9. The device according to claim 8, wherein said R/W selectors have first outputs connected to respective said first global bitlines and second outputs connected to respective said second global bitlines.

10. The device according to claim 8, further including:

a first column decoder, arranged between said first global bitlines and said first sense amplifiers, and a second column decoder, arranged between said second global bitlines and said second sense amplifiers.

11. The device according to claim 1, further including:

a control unit having first outputs, connected to said first sense amplifiers and supplying first driving signals and first reference signals, second outputs connected to said second sense amplifiers and supplying second driving signals and second reference signals, and a third output supplying a timing signal.

12. The device according to claim 11, wherein said second driving signals are synchronous with said timing signal.

13. An integrated memory array that provides simultaneous reading and writing to individual memory cells within the array, comprising:

at least two memory banks within said array, each memory bank having a plurality of memory cells therein and both memory banks being adjacent to each other on the same integrated circuit;

a set of global output bit lines coupled to each memory bank;

a set of global verify bit lines coupled to each bank of the memory array;

a read address decoder circuit coupled to address a memory cell within each bank of the memory array to permit reading of a memory cell within the array; and

a verify address decoder circuit coupled to address a memory cell with the bank of the memory array to permit verifying the status of data during a write operation within each memory bank.

14. The integrated circuit according to claim 13 wherein the read address decoder and the verify address decoder are completely independent from each other in structure for each memory bank of the array.